## What is claimed is:

[Claim 1] 1. A method of fabricating a flash memory cell, comprising the following steps:

providing a substrate;
forming a first opening and a second opening in the substrate, wherein the second opening is formed on the bottom of the first opening, the second opening is narrower but is deeper, as measured from the surface of the substrate, than the first opening;
forming a high-voltage doped region under the bottom of the second opening in the substrate;
forming a gate dielectric layer on the substrate in the first opening and the second opening;
forming a first conductive spacer on a sidewall of the first opening as a select gate, and forming a second conductive spacer on a sidewall of the second opening as a floating gate; and
forming a source region beside the first opening in the substrate.

[Claim 2] 2. The method of fabricating a flash memory cell of claim 1, wherein the step of forming the first opening comprises:

forming a mask layer with the pattern of the first opening over the substrate; and
etching the substrate with the mask layer as mask to form the first opening.

[Claim 3] 3. The method of fabricating a flash memory cell of claim 2, wherein the first opening has round corners on its bottom.

[Claim 4] 4. The method of fabricating a flash memory cell of claim 2, wherein the step of forming the second opening comprises:

forming spacers on the sidewalls of the mask layer and the first opening; and
etching the substrate, with the mask layer and the spacers as mask, to form the second opening.

[Claim 5] 5. The method of fabricating a flash memory cell of claim 4, wherein the second opening has round corners on its bottom.

[Claim 6] 6. The method of fabricating a flash memory cell of claim 4, wherein the process to form the high-voltage doped region under the bottom of the second opening in the substrate comprises a step of ion implantation, with the mask layer and the spacer as mask, to the substrate.

[Claim 7] 7. The method of fabricating a flash memory cell of claim 1, wherein the process to form the gate dielectric layer on the surface of the substrate in the first opening and the second opening comprises thermal oxidation.

[Claim 8] 8. The method of fabricating a flash memory cell of claim 1, wherein the process to simultaneously form the first and the second conductive spacers comprises:

forming a conformal conductive layer on the substrate; and
anisotropic etching the conformal conductive layer to form the first conductive spacer on the sidewalls of the first opening and the second opening.

[Claim 9] 9. The method of fabricating a flash memory cell of claim 8, wherein the materials of the conformal conductive layer comprise polysilicon.

[Claim 10] 10. The method of fabricating a flash memory cell of claim 1, the method further comprises:

forming an insulating layer on the substrate, where the insulating layer covers the select gate and the floating gate; and
forming a contact plug which penetrates through the insulating layer and is electrically connected with the high-voltage doped region.

[Claim 11] 11. The method of fabricating a flash memory cell of claim 10, the method further comprises a step, before the formation of the insulating layer, to form an insulating spacer on another sidewalls of the select gate and the floating gate so as to protect the floating gate in the process of forming the contact plug.